REMARKS

Present Status of the Application

The Office Action mailed August 11, 2003 rejected all presently pending claims 1-16 and 19-21. Specifically, claims 1-16 and 19-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al (US 6,118,154) in view of Hu el al. (US 6,121,077) and Japanese Patent #4-76959. In response thereto, Applicants have further amended independent claims 1, 9, 14 and 21. No new matter adds through the amendments. Reconsideration of claims 1-16 and 19-21 is respectfully requested.

Discussion of Amendments

The limitation "wherein the single crystal Si resistors (or single resistors) are arranged in parallel connection" newly added to independent claims 1, 9, 14 and 21 is fully supported by the original disclosure (for example, see FIG. 3 and page 6, lines 4-5 and lines 20-21). More specifically, FIG. 3 illustrates multiple single crystal Si lines (resistors) 308 that are arranged in parallel, while each single crystal Si resistor 308 is electrically connected to the same metal layer 314 via a plug 310. Therefore, the single crystal Si resistors 308 are arranged in parallel connection.

Discussion of Office Action Rejections

One feature of this invention is that the single crystal Si resistors (or single resistors) of an input resistor are arranged in ***parallel connection. The feature is recited in amended independent claims 1, 9, 14 and 21 as above,*** marked by underlines.

Yamaguchi et al. fail to teach or suggest the above feature of claims 1, 9, 14 and 21, since

the two single crystal silicon resistors 36 and 37 of the input resistor in Yamaguchi et al. are arranged in ***series connection***, as clearly shown in FIG.19, which is obviously different from ***parallel connection***. The above feature of the invention is not disclosed in Hu el al. and Japanese Patent #4-76959 either. Therefore, at least the above feature of this invention cannot be obtained by combining Yamaguchi et al., Hu el al. and Japanese Patent #4-76959.

Moreover, the above feature is ***not merely a simple change from the series connection in the prior art to parallel connection***. The input resistor constituted of multiple single resistors 308 arranged in parallel connection as shown in FIG. 3 is equivalent to the resistor 102 as shown in FIG. 1. By comparing FIG. 1 of this application and FIG. 19 of Yamaguchi, the input resistor constituted of multiple single resistors 308 arranged in parallel connection of this invention may be equivalent to the left resistor 36 of Yamaguchi only. Therefore, the above feature of this invention is structurally different from the resistors 36 and 37 in series connection. In Yamaguchi, it is required that input resistance 36 be wider than internal resistance 37 so that the current density of input resistance 36 is reduced. Col. 6, line 49-51. There is no such requirement for resistors 308 of the present invention.

Furthermore, an input resistor constituted of multiple single resistors in parallel connection (referred as a resistor of type-I hereinafter) has many advantages over one constituted of a single resistor only. For example, the resistance of a resistor of type-I can be easily adjusted by varying the number of single resistors, and a resistor of type-I is not easily damaged by an ESD current since the ESD current can be distributed to multiple single resistors. Accordingly, the above feature of this invention is not merely a trivial modification of the prior art.

For at least the reasons mentioned above, Applicants respectfully submit that amended independent claims 1, 9, 14 and 21 patently define over the prior art.

For at least the same reasons mentioned above, Applicants respectfully submit that claims 2-8 dependent from claim 1, claims 10-13 from claim 9, claims 15-16 and 19-20 from claim 14 also patently define over the prior art.

CONCLUSION

For at least the forgoing reasons, it is believed that all pending claims 1-16 and 19-21 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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